

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application

Inventors: OM P. AGRAWAL et al.

Serial No.: 09/235,615

Filed: January 21, 1999

Title: FPGA INTEGRATED CIRCUIT HAVING EMBEDDED  
SRAM MEMORY BLOCKS WITH REGISTERED  
ADDRESS AND DATA INPUT SECTIONS



) PATENT APPLICATION

) Art Unit: 2819

**CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8**

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Gideon Gimlan, Esq., Reg. No. 31,955 (Attorney Signature)  
Signature Date: February 24, 1999

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Sir:

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It is hereby respectfully requested that the Patent Office correct its records to indicate a filing date of January 21, 1999 and issue a corrected Filing Receipt.

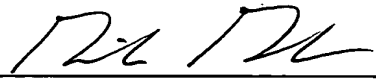
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FLIESLER, DUBB, MEYER & LOVEJOY  
Four Embarcadero Center, Suite 400  
San Francisco, California 94111-4156  
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Respectfully submitted,

By:   
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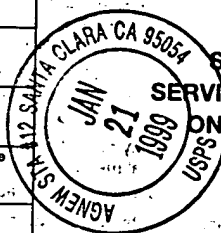


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